Notice of References Cited

Application/Control No. 10/084,367	Applicant(s)/Pate Reexamination NANJO ET AL.		
Examiner	Art Unit		
Toniae M. Thomas	2822	Page 1 of 1	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-4,622,735 B1	11-1986	Shibata	438/143
	В	US-5,610,088 B1	03-1997	Chang et al.	438/231
	С	US-5,780,350 B1	07-1998	Kapoor	438/305
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	Н	US-			
	1	US-			
	J	US-			
	К	US-			
	L	US-			
	М	US-			

FOREIGN PATENT DOCUMENTS

	FORLIGN FATENT DOCUMENTS					
*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					
	Φ					
	ď					
	R					
	S					
	Т					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)				
	U	Wolf, Ph.D., Stanley, "CMOS Process Integration," Silicon Processing for the VLSI Era: Vol. 2 - Process Integration, Lattice Press, 1986, pages 428-431.				
	V					
	w					
	х					

"A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.